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(54) A phase comparator

(57) A phase comparator comprises a circuit 1 producing first and second pulse trains at 2d, 3d of pulse widths respectively corresponding, to the intervals between corresponding zero crossings in a positive-going direction and in a negative-going direction of two alternating signals S1, S2, a further circuit 8 producing a signal indicative of the relative phase lead/lag relationship of S1, S2, an arrangement 10 for selectively gating one of the pulse trains at 2d, 3d with a polarity depending upon the output of circuit 8 and an integrator 15 producing a dc signal whose magnitude and polarity are representative of the phase difference detected.

The comparator is less sensitive to changes in signal frequency and amplitude, supply variations, ambient temperature etc and is effective over a range greater than 100° of phase differences. The comparator may optionally limit the output at a higher preset maximum phase difference.

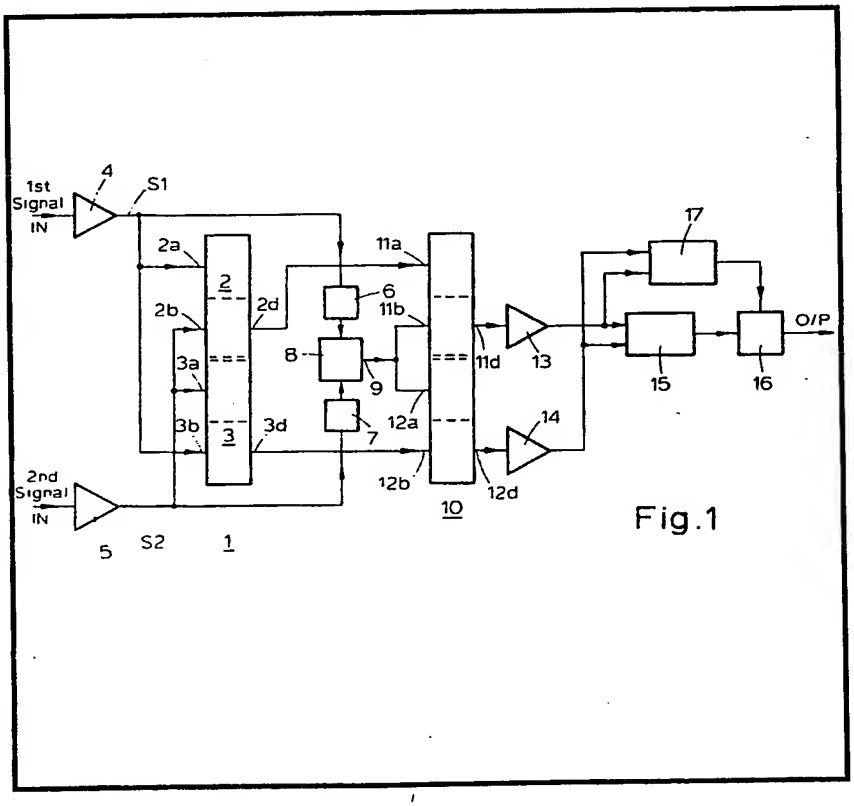

Fig.1

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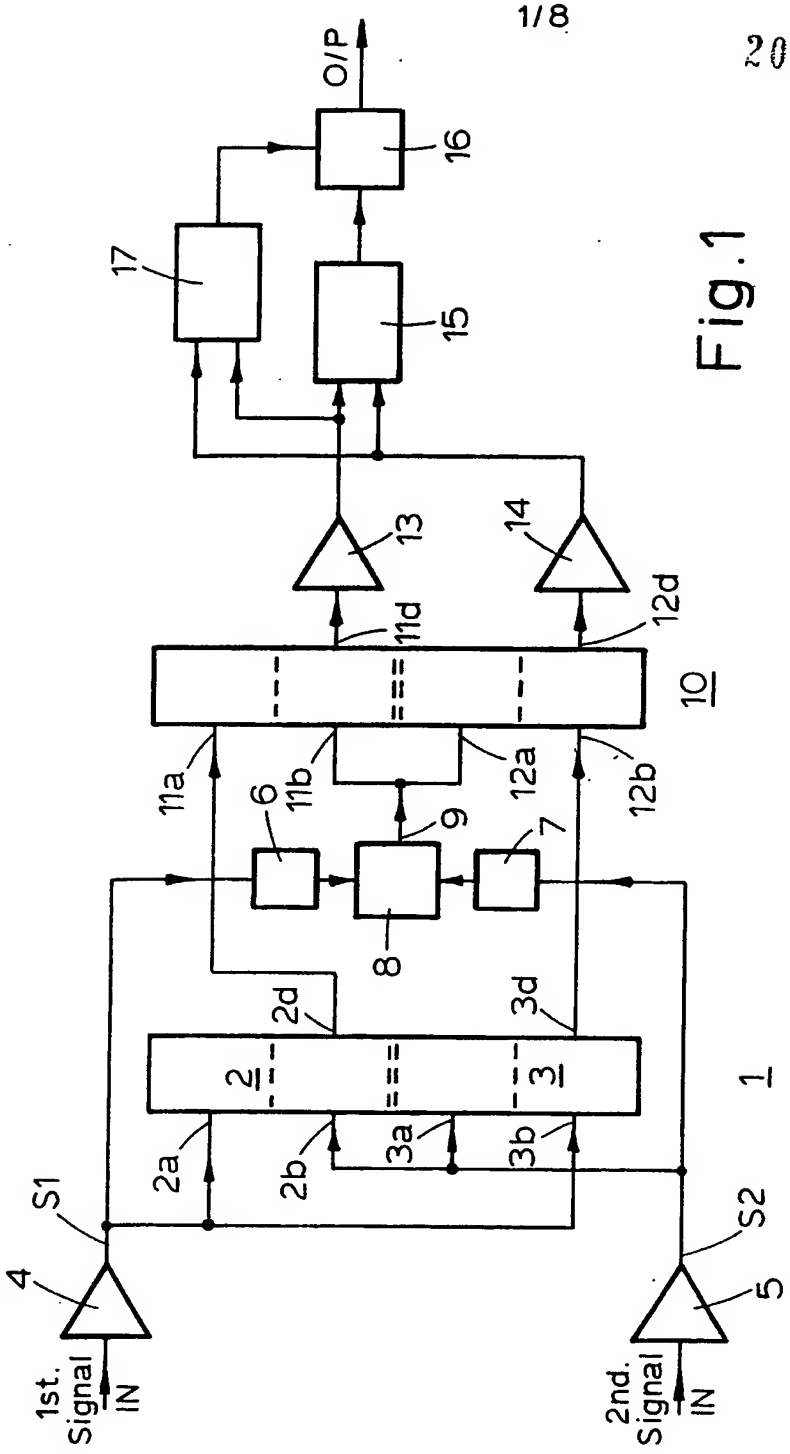

Fig.1

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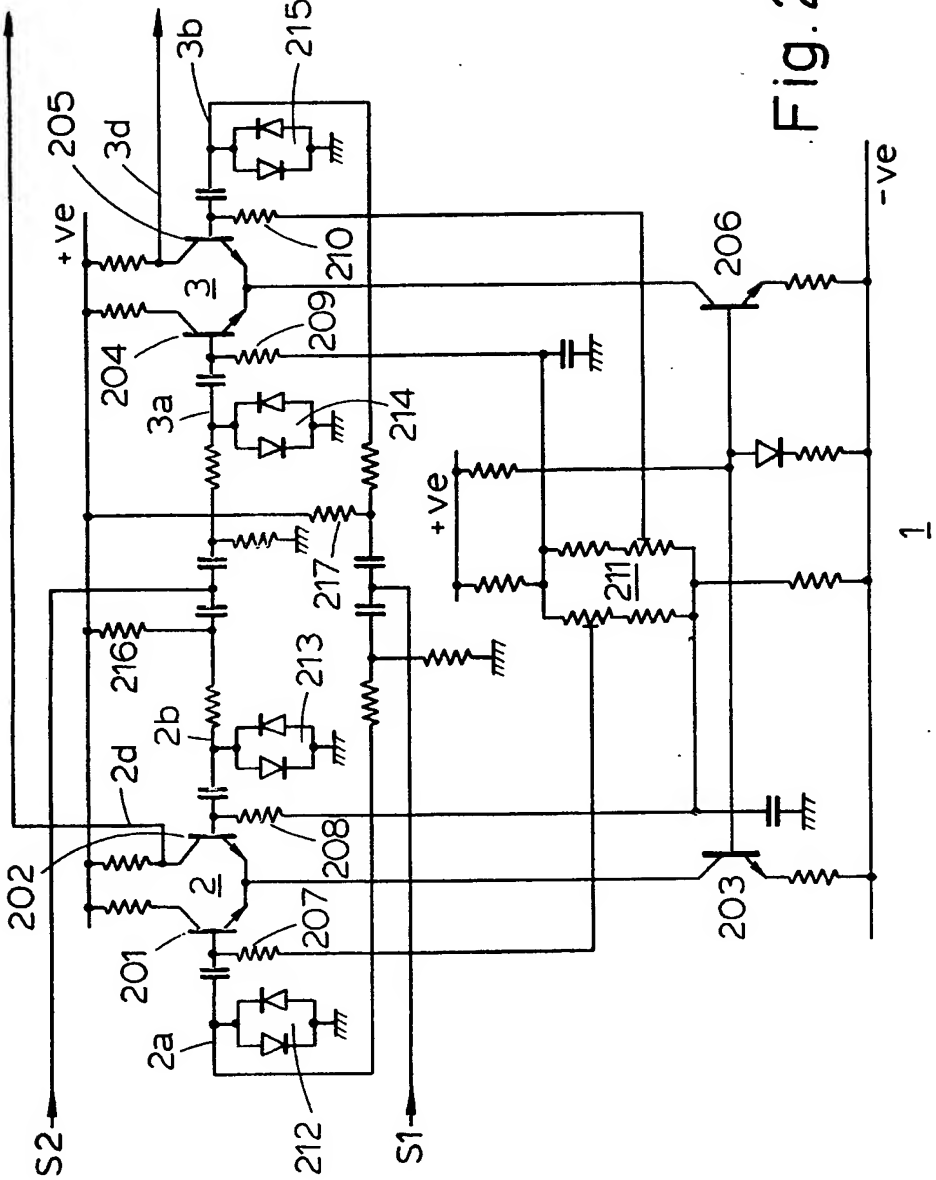

Fig. 2

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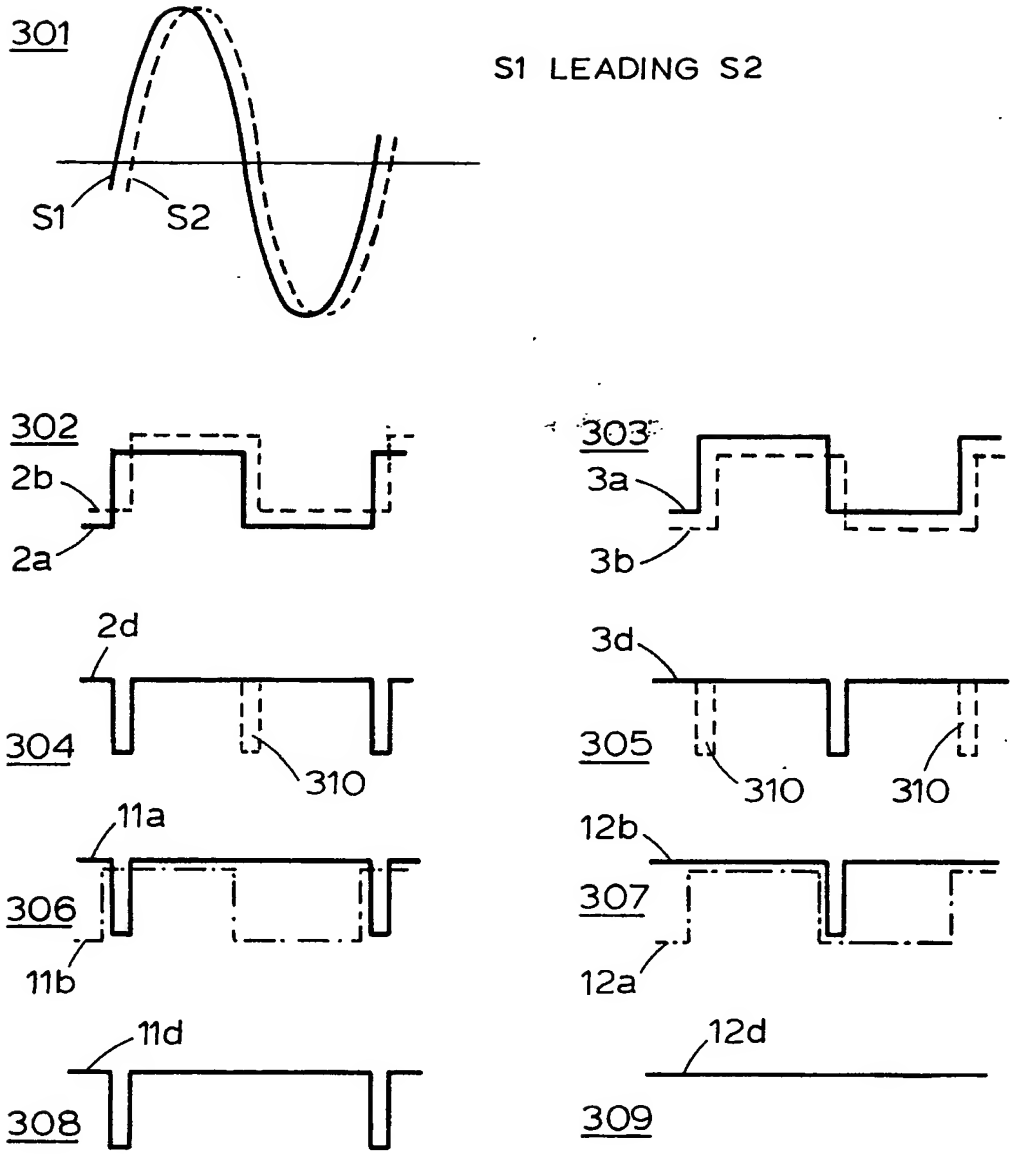

Fig. 3

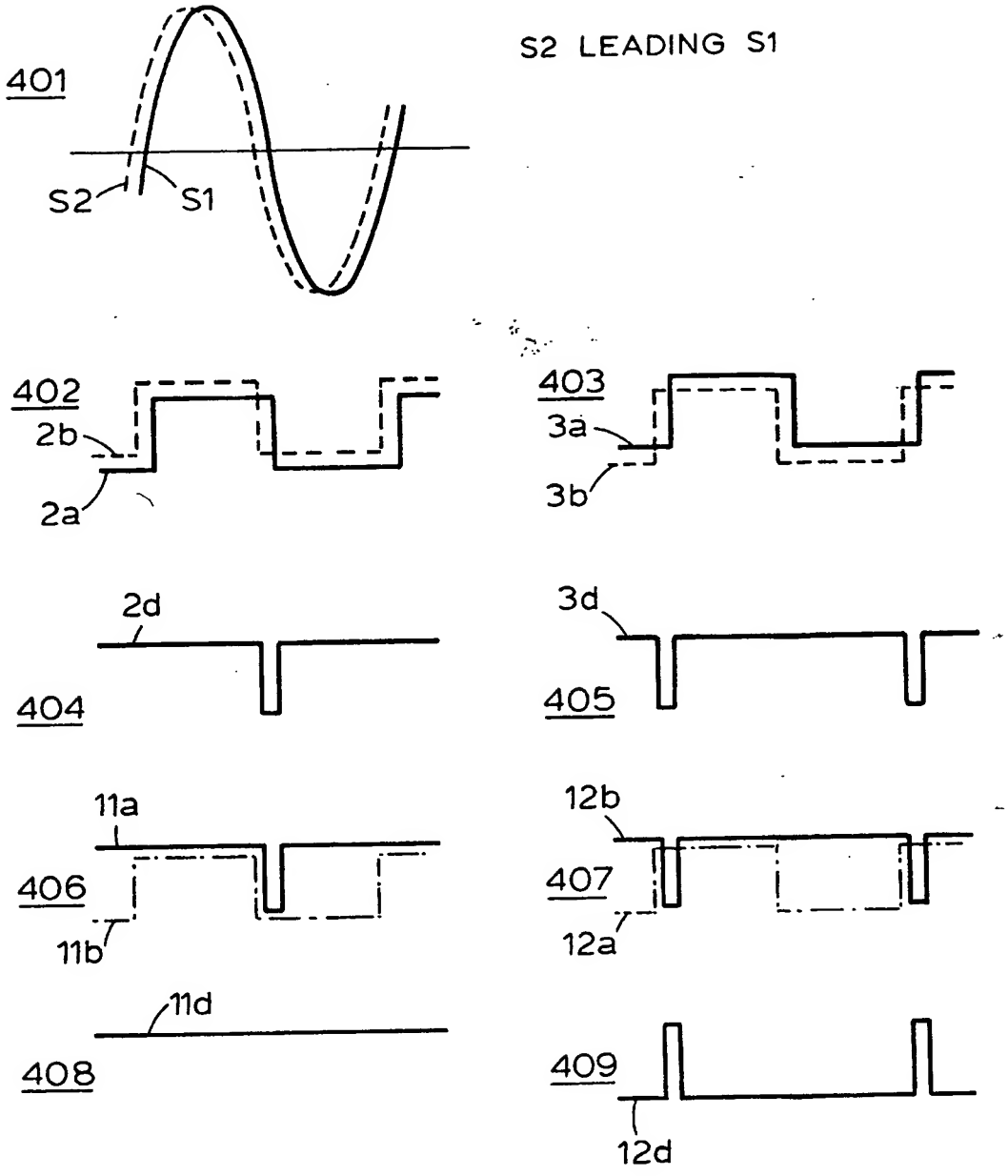
S2 LEADING S1
401
S2
S1
402
2b
2a
403
3a
3b
2d
404
3d
405
11a
406
11b
12b
407
12a
11d
408
409
12d

Fig.4

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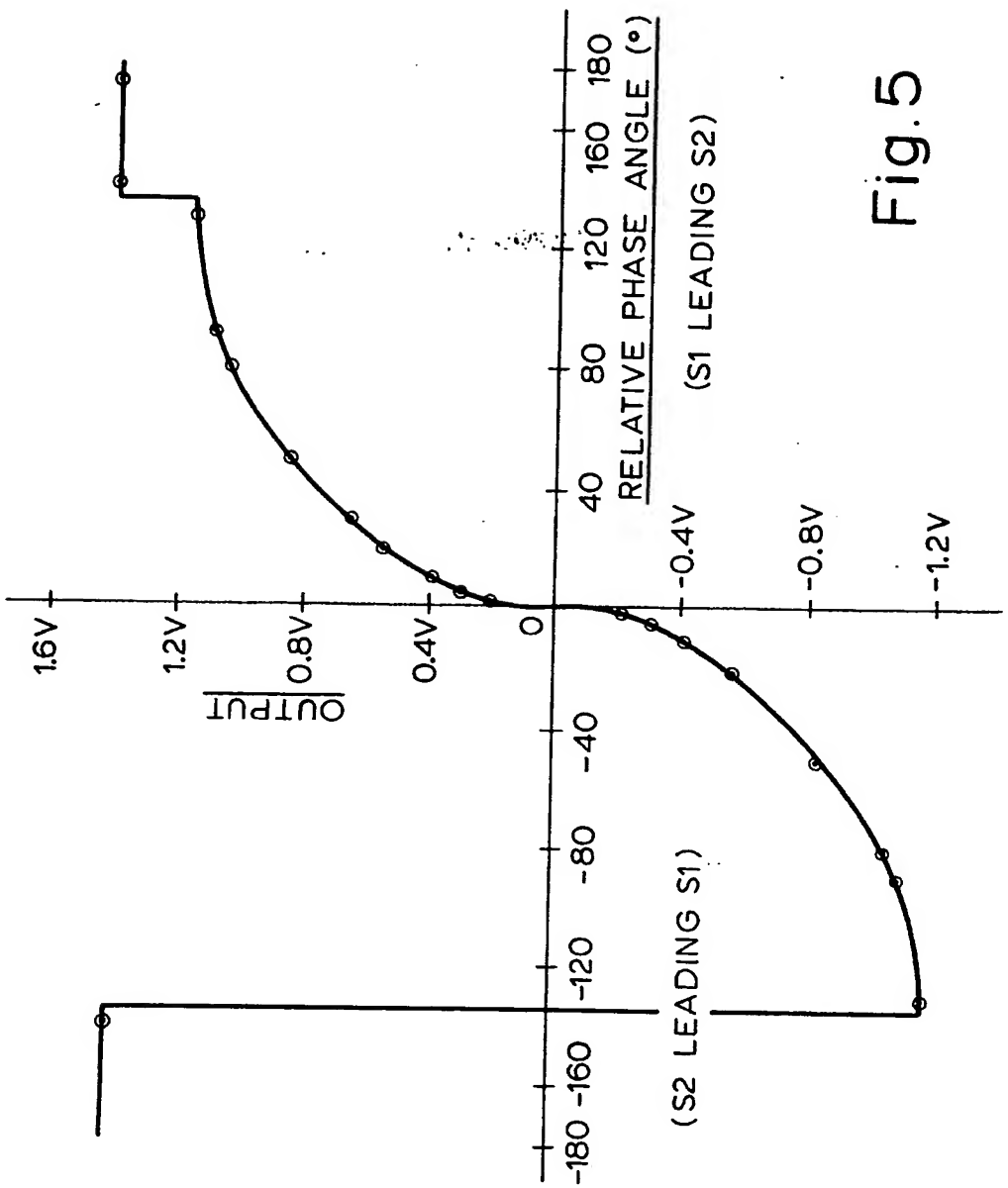

Fig.5

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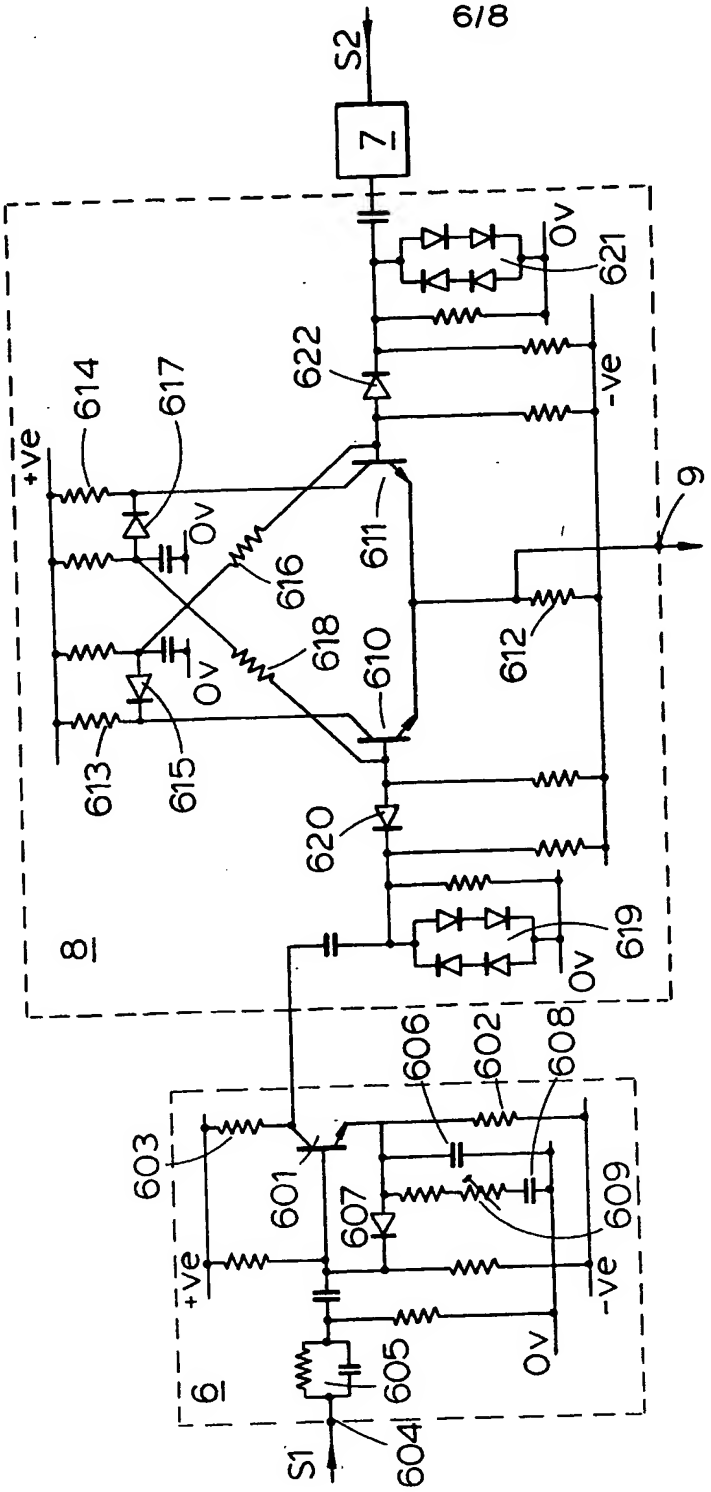

Fig. 6

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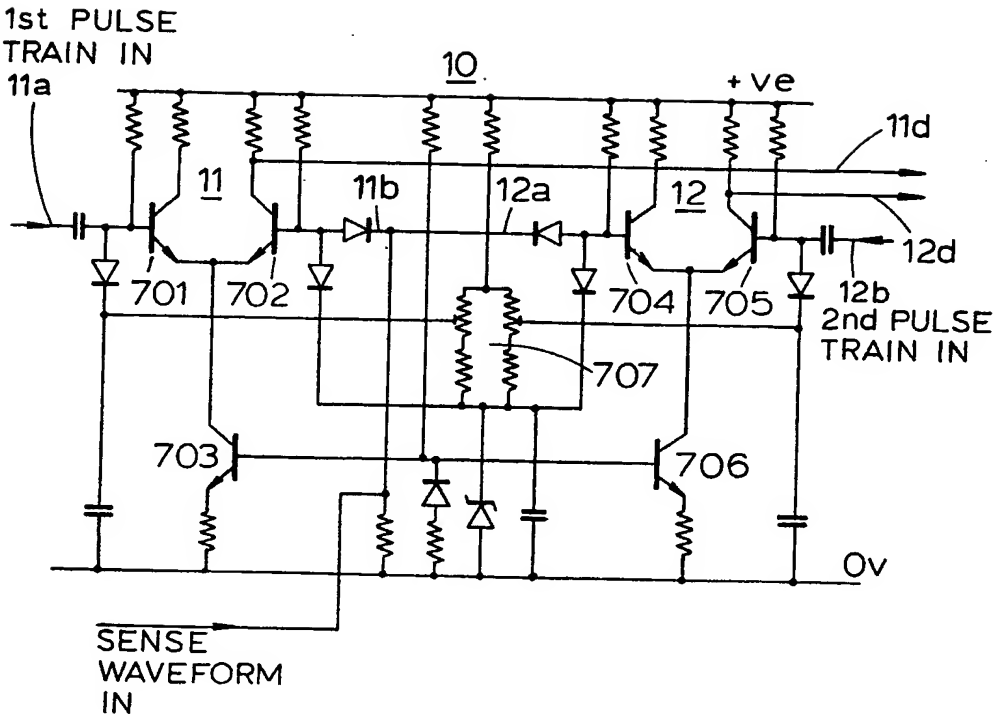

Fig. 7

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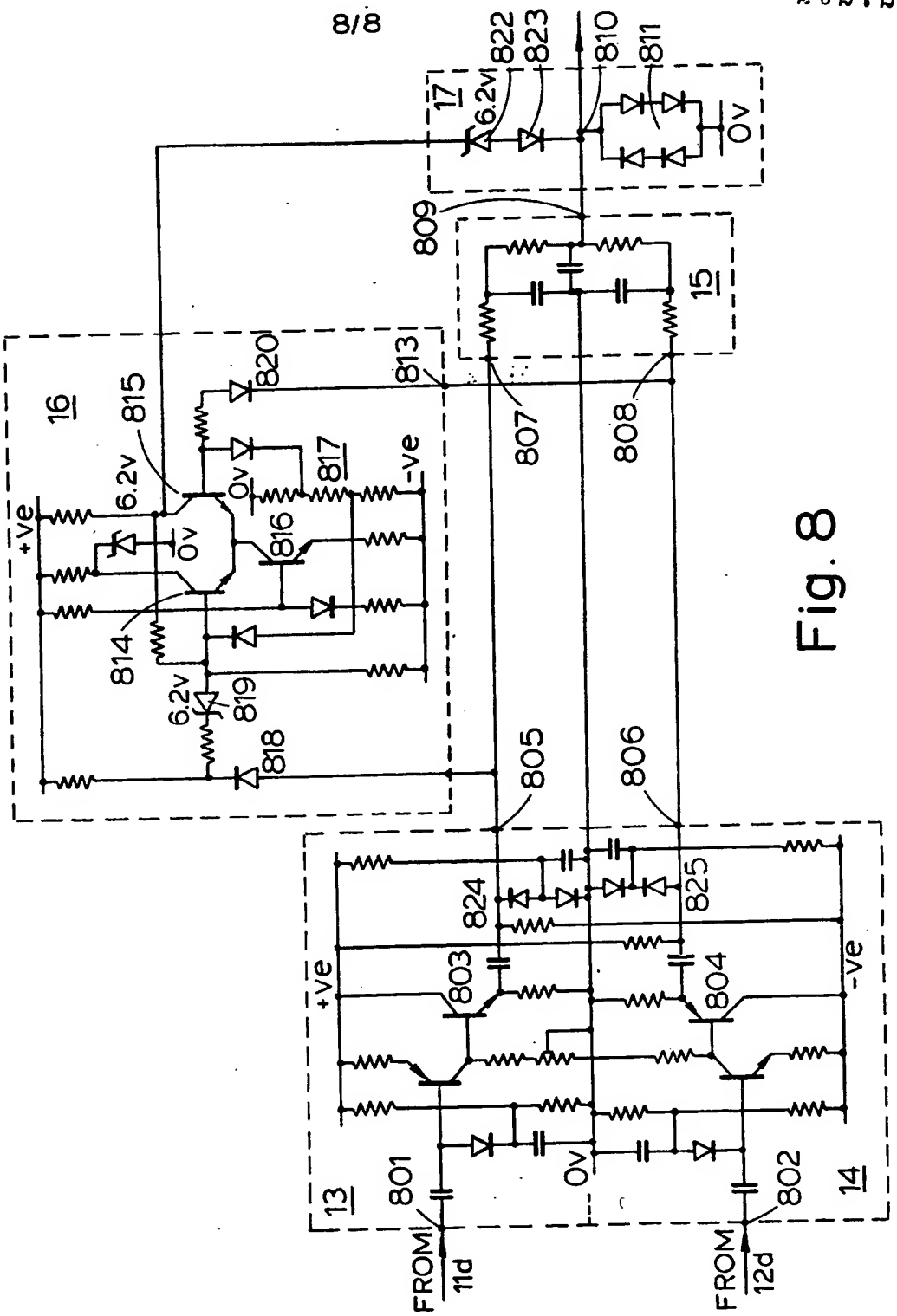

Fig. 8

SPECIFICATION

Phase comparison apparatus

The present invention relates to apparatus for measuring the phase difference between two alternating signals. It has particular application in colour television transmission systems.

In colour television systems in which colour signals are modulated on a colour subcarrier whose frequency bears a specified relationship to the line frequency, it is the practice to provide an oscillator operating at the subcarrier frequency and to derive from the output of this oscillator all the waveforms required for the control of cameras and modulating equipment, together with the combined (horizontal, vertical and subcarrier burst) synchronising signals which are transmitted with the picture signals.

The assembly comprising a subcarrier oscillator and the various devices such as frequency dividers, multipliers, modulators etc used to produce the control and synchronising waveforms may be referred to collectively as a synchronising generator unit (hereinafter SGU).

A colour television transmitter, in addition to transmitting pictures derived from local or studio cameras controlled by a local SGU, may be required to transmit pictures derived from a remote camera which is controlled by a remote SGU. Such requirements arise, for example, when it is desired to change from a studio camera to an outside broadcast camera.

It is required that all mixing techniques, eg. fading, rolling cut, chroma keying, etc which may be used when changing from one local camera to another should also be available when changing from a local to a remote camera or vice versa. This requires that the local SGU by synchronised with the remote SGU and in particular that the subcarrier burst component of the locally-produced combined video/synchronising signal be synchronised in frequency and phase to a high degree of accuracy, with the subcarrier burst component of the combined video/synchronising signal received at the local site from the remote equipment.

To this end, it is customary to use the respective subcarrier burst components of the local and remote combined video/synchronising signals to control, by means of respective phase-locked loops, first and second oscillators, hereinafter referred to as transfer oscillators, so that the first transfer oscillator produces a continuous sinusoidal signal (the first transfer signal) substantially equal in frequency and phase to the burst component of the local combined video/synchronising signal and the second transfer oscillator produces a second transfer signal substantially equal in frequency and phase to the subcarrier burst component of the remote video/synchronising signal as received at the local site.

The first and second transfer signals are applied to respective inputs of a phase comparator circuit arranged to produce an output signal representative in magnitude and sign of any phase difference between the first and second transfer signals. The output signal is applied to control the phase of the local subcarrier oscillator, and therefore the phases of the local subcarrier burst component and the first transfer signal in such a manner as to minimise any phase error between the first and the second transfer signals. Consequently the local subcarrier burst component becomes synchronised in frequency and phase with the remote subcarrier burst component received at the local site.

It is desirable that the phase comparator circuit should have an accuracy of at least $\pm \frac{1}{4}°$ and that its stability over small changes of input signal level, component parameters, ambient air temperature or supply voltage variations should be within $\pm \frac{1}{2}°$.

Phase comparators previously used in the synchronisation of television SGU's have been of the so-called "False Quadrant" type. In this type of comparator, in order to remove ambiguity as to which of the two input signals leads the other, one of the input signals is phase shifted by 90° before it is applied to a first input of a double-balanced phase comparison circuit, the other input signal being applied without phase shift to a second input of the comparison circuit. The comparison circuit itself is a double-balanced phase detector of the type comprising two long-tailed pair circuits which may conveniently be provided in the form of an integrated circuit such as the Fairchild Type uA796 or the Mullard Type TCA240.

Difficulty is found with False Quadrant comparators in meeting the requirements for accuracy and stability. Such comparators are frequency sensitive, in consequence of the requirement for phase shifting of one input signal. In general the shift produced by the phase shift network will be frequency dependent and will equal 90° only at one specifical frequency, which will be liable to change with variations in component parameters, ambient air temperature, etc. It will be appreciated that any error in the 90° phase shift of one input signal to a False Quadrant phase comparator will produce a corresponding error in the measurement of phase difference between the two signals. Moreover, False Quadrant phase comparators can operate over only a limited range of phase differences ($\pm \pm 90°$).

It is an object of the present invention to provide a phase comparator (for use in the synchronising of colour television transmission systems) for comparing the phases of two sinusoidal signals which provides greater accuracy and is less susceptable to error due to

changes in component parameters, ambient air temperature, supply voltages and input signal levels than the previously-used phase comparator and which can measure phase differences over a range $> \pm 100°$.

Apparatus for comparing the phases of first and second alternating signals according to the present invention comprises comparator means for producing a first pulse train of which successive pulses correspond in width to the time intervals between corresponding zero crossings in a first sense of successive cycles of the first and second signals, and a second pulse train of which successive pulses correspond in width to the time intervals between corresponding zero crossings in an opposite sense of successive cycles of the first and second signals, the pulses of the first pulse train and the pulses of the second pulse train being of equal amplitudes and the same polarity, means for generating a substantially square sense waveform corresponding in phase to the one of the first and second signals which is leading in phase, means for gating the first pulse train and the second pulse train by the sense waveform to produce a gated first pulse train only when the phase of the first signal is in advance of the phase of the second signal and to produce a gated second pulse train having pulses of polarity opposite to the pulses of the gated first pulse train only when the phase of the second signal is in advance of the phase of the first signal and means for integrating either the pulses of the gated first pulse train or the pulses of the gated second pulse train to produce a d.c. output signal whose magnitude and polarity are representative respectively of the magnitude and sense of the phase difference between the first and second signals.

The comparator means may comprise a first and a second long-tailed pair transistor circuit so arranged that under no-signal conditions a first transistor of the first pair and a first transistor of the second pair are conducting, a second transistor of the first pair and a second transistor of the second pair being non-conducting, the first alternating signal being connected to the respective base electrodes of the first transistor of the first pair and the second transistor of the second pair, the second alternating signal being connected to the respective base electrodes of the second transistor of the first pair and the first transistor of the second pair, the first pulse train being obtained at a collector electrode of the second transistor of the first pair and the second pulse train being obtained at a collector electrode of the second transistor of the second pair.

The means for generating the sense waveform may comprise a bistable circuit having first and second trigger inputs, a first trigger signal corresponding to the first alternating signal being connected to the first trigger input and a second trigger signal corresponding to the second alternating signal being connected to the second trigger input, the arrangement being such that when the circuit is set to a particular state by a transition in one sense of either one of the trigger signals, it remains in that state until reset to its other stable state by a transition in the opposite sense of the same trigger signal, irrespective of any changes in the other trigger signal in the intervening period.

There may be provided means for advancing the phase of the first trigger signal with respect to the phase of the first alternating signal and means for advancing the phase of the second trigger signal with respect to the phase of the second alternating signal.

The means for gating the first pulse train and the second pulse train with the sense waveform may comprise a first and a second long-tailed pair transistor circuit so arranged that under no-signal conditions a first transistor of the first pair and a second transistor of the second pair are conducting, a second transistor of the first pair and a first transistor of the second pair being non-conducting, the first pulse train being connected to a base electrode of the first transistor of the first pair, the second pulse train being connected to a base electrode of the second transistor of the second pair and the sense waveform being connected to respective base electrodes of the second transistor of the first pair and the first transistor of the second pair, the gated first pulse train being obtained at a collector electrode of the second transistor of the first pair and the gated second pulse train being obtained at a collector electrode of the second transistor of the second pair.

Means may be provided for detecting the simultaneous occurrence of pulses of the gated first pulse train and of the gated second pulse train and for over-riding the output signal from the integrator means when such simultaneous pulses are detected.

In order that the invention and the manner in which it is to be performed may be fully understood, an embodiment thereof will now be described with reference to the accompanying drawings, of which:—

Figure 1 is a block schematic diagram of apparatus according to the invention

Figure 2 is a more detailed schematic diagram of a comparator unit for use in the arrangement of Fig. 1

Figure 3 and 4 illustrate waveforms occurring at various points in the apparatus of Fig. 1

Figure 5 is a graph showing output versus phase difference for the apparatus of Fig. 1

Figure 6 is a more detailed schematic diagram of a sense waveform generator for use in the apparatus of Fig. 1

Figure 7 is a more detailed schematic diagram of gating means for use in the apparatus

of Fig. 1, and

Figure 8 is a more detailed schematic diagram of integrating means and double-pulse detection means for use in the apparatus of Fig. 1.

Referring first to Fig. 1, in which the embodiment is illustrated in block schematic form, a comparator unit indicated generally by the reference numeral 1 comprises two long-tailed pair transistor circuits 2 and 3. A first input signal is amplified at 4 and the amplified signal S1 is applied to an input 2a of the pair 2 and an input 3b of the pair 3. A second input signal is amplified at 5 and the amplified signal S2 is applied to respective inputs 2b and 3a of the pairs 2 and 3.

As will be described in greater detail hereinafter with reference to Fig. 2, the comparator unit 1 produces at respective output terminals 2d and 3d of the pairs 2 and 3, first and second pulse trains. The pulses of both pulse trains are of equal amplitude, but the pulses of the first pulse train correspond in width to the interval between corresponding zero crossings in one sense of the signals S1 and S2. Similarly the pulses of the second train correspond in width to the intervals between corresponding zero crossings in the opposite sense of the signals S1 and S2. The widths of the pulses of both trains are thus representative of the magnitude of the phase difference between the signals S1 and S2, the pulses of the second train occurring mid-way between the pulses of the first train. The signals S1 and S2 are also applied, via respective phase advance units 6 and 7 to inputs of a sense waveform generator unit 8 which produces at its output 9 a substantially square sense waveform corresponding to the one of the signals S1 and S2 which is leading in phase. The phase advance units 6 and 7 are provided so that the edges of the sense square wave signal lead the pulses of the first and second pulse trains, so that the sense signal may be effective to gate the said pulse trains.

The units 6, 7 and 8 are described in greater detail hereinbelow with reference to Fig. 3.

A gate unit 10 comprises two long-tailed pair transistor circuits 11 and 12. The first pulse train appearing at the output 2d of the comparator unit 1 is applied to an input 11a of the pair 11. The second pulse train appearing at the output 3d is applied to an input 12b of the pair 12. The sense waveform appearing at the output 9 of the sense waveform generator unit 8 is applied to respective inputs 11b and 12a of the pairs 11 and 12. Output signals are taken from the output 11d of the pair 11 and output 12d of the pair 12. As will be described hereinbelow with reference to Fig. 4, the arrangement is such that when the signal S1 leads S2, a signal corresponding to the first pulse train appears at the output 11d, and no signal appears at the output 12d. When S2 leads S1, no signal appears at 11d but a signal corresponding to the second pulse train appears at 12d. Moreover, signals which may appear at 12d are of opposite polarity to those which may appear at 11d.

The pulse signals appearing at the output 11d and 12d of the gate unit 10, after amplification by respective amplifiers 13 and 14 are applied to respective inputs of an integrator unit 15. In general, pulses of one polarity are applied to the integrator unit 15 when the phase difference between the signals S1 and S2 is of one sense, and pulses of the opposite polarity when the phase difference is of the opposite sense. The output of the unit 15 is therefore a dc signal whose magnitude and polarity are representative respectively of the magnitude and sense of the phase difference.

For very large phase differences (typically $> \pm 150°$) it may occur that the transitions of the sense waveform fall within the pulses of the first and second pulse trains. The gate unit 10 will then produce output pulses simultaneously at both its outputs 11d and 12d (double-pulse condition). Moreover the widths of such pulses will no longer correspond to the magnitude of the phase difference between the input waveforms. Under double-pulse conditions, therefore, the output signal from the integrator unit 15 will be ambiguous.

To prevent any ambiguity in the system output signal, the output of the integrator unit 15 is applied to an input of a limiter circuit 16 arranged to clip the signal at positive and negative values corresponding to phase differences (typically $\pm 135°$) somewhat lower than the phase differences at which double-pulsing commences. A double-pulse detector unit 17 has respective inputs connected to the outputs of the amplifiers 13 and 14, and an output connected to the input of the limiter 16. The unit 17 is adapted to produce a dc output signal when and only when pulses exceeding a preset level are present at both its inputs, ie. in the double-pulse condition, the output signal then being of magnitude sufficient to hold the output of the limiter unit at one of its limit values regardless of the magnitude and polarity of the integrator output. For phase differences greater than say $\pm 135°$, the system output is therefore held constant at a value corresponding to $\pm 135°$.

Units of the present embodiment will now be described in greater detail. The comparator unit 1 is illustrated by Fig. 2. It will be seen that the unit comprises transistors 201 and 202 arranged as a first long-tailed pair 2 having a tail transistor 203 and transistors 204 and 205 arranged as a second long-tailed pair 3 having a tail transistor 206, the transistors 203 and 206 being arranged to serve as constant current sources for their

respective pairs. The bases of the transistors 201, 202, 204, and 205 are connected via respective resistors 207 to 210 to tappings on a potential divider chain connected between positive and negative supply rails and indicated generally by the reference numeral 211 such that under no-signal conditions the first half of each pair (ie transistors 201 and 204) is conductive and the second half of each pair (ie transistors 202 and 205) is cut off. The transistors 201–206 inclusive may conveniently be provided in an integrated circuit such as the Type CA3054 manufactured by R.C.A.

The amplified signal S1 is applied through suitable dc blocking capacitors and series resistors to the bases of transistors 201 and 205, and the amplified signal S2 is similarly applied to the bases of transistors 202 and 204. Clipping circuits 212–215, each comprising a pair of oppositely-poled diodes are connected to clip the signal waveforms applied to the respective transistor bases to a substantially square wave shape having an amplitude less than the transistor base/emitter voltage rating.

Considering the first long-tailed pair, pulse signals (the first pulse train) appear at the collector of transistor 202 (output 2d) equal in width to the time interval between corresponding edges of the square wave signals applied to the bases of transistors 201 and 202. The width of the pulses is thus a measure of the phase difference between the waveforms S1 and S2.

The biassing of the transistors ensures that the pulses are of one polarity, i.e. only one pulse is formed per cycle of the input waveforms.

Similar considerations apply to the second long-tailed pair, but since this pair is biassed in the opposite sense to the first, the pulses appearing at the collector of transistor 205 (output 3d) are 180°, i.e. the second pulse train, are 180° out of phase with the pulses of the first train.

The operation may be more clearly understood from consideration of the waveforms shown in Fig. 3, drawn for the case where S1 leads S2, and Fig. 4 drawn for S2 leading S1.

Referring to Fig. 3, corresponding cycles of S1 (full line) and S2 (dashed) with S1 leading S2 are shown at 301. The resulting waveforms at the inputs to the first long-tailed pair 2 are shown at 302 and the inputs to the second long-tailed pair at 303. The waveform at the output 2d of the first long-tailed pair is shown at 304 and the waveform at the output 3d of the second long-tailed pair at 305. Note that the threshold biassing of the two long-tailed pairs prevents the production of pulses as shown dotted at 310. It will be seen that pulses of the second pulse train (305) are 180° out of phase with those of the first pulse train (304), but that the pulses of both trains are of constant amplitude and of width corresponding to the phase difference between the input waveforms S1 and S2. Fig. 4 shows the corresponding waveforms 401–405 for the case where S2 leads S1.

To avoid loss of sensitivity near the "in-phase" condition, when the pulses of the first and second trains become very narrow and of reduced amplitude due to the finite rise time of the input waveforms the diode clipper circuit 213 associated with the right hand half (as shown in Fig. 2) of the first long-tailed pair 2 is biassed through a resistor 216 connected to the positive supply rail and the diode clipper 215 associated with the right hand half of the long tailed pair 3 is biassed through a resistor 217 connected to the negative supply rail. The waveforms applied to the inputs of the two long-tailed pairs are therefore slightly assymetric.

Consequently, small pulses appear at the outputs 2d and 3d even when the input waveforms S1 and S2 are in phase. As can be seen from the system response curve Fig. 5, this leads to high sensitivity in the region of zero phase difference.

The phase advance units 6 and 7 and the sense waveform generator unit 8 are illustrated by Fig. 6. The pulse advance unit 6 is shown within the broken rectangle 6 and is of known form, comprising an n.p.n. transistor 601. The emitter of transistor 601 is connected to the negative supply rail via a resistor 602 and its collector is connected to the positive supply rail via a resistor 603. An output signal is taken from the collector of transistor 601.

The amplified input signal S1 is applied to an input terminal 604 which is connected via an impedance network 605 to the base of the transistor 601. A capacitor 606 is connected between the emitter of the transistor 601 and ground. It will be seen that energy stored in the capacitor 606 during any one cycle of the input waveform S1 will be fed to the base of the transistor 601 via a diode 607 during the next succeeding cycle, and consequently the phase of the output signal at the collector of the transistor 601 will be advanced relative to the signal at the input terminal 604, by an amount dependent on the energy stored in the capacitor 606. To allow adjustment of the amount of energy stored, and hence of the degree of phase advance, a further capacitor 608 in series with a variable resistor 609 may be connected across the capacitor 606. In the case of a phase comparator for input signal frequencies of 4.43MHZ ie. the PAL colour subcarrier frequency, the degree of phase advance required is of the order of some 20 nanoseconds, equivalent to about 32°.

The phase advance unit 7 is identical to the unit 6 and need not be further described herein.

The sense waveform generator unit is shown within the broken rectangle 6, and comprises transistors 610 and 611 having their emitters connected together and to the negative supply rail via a common emitter resistor 612. The collectors of the transistors 610 and 611 are connected to the positive supply rail via respective resistors 613 and 614. The collector of the transistor 610 is further dc connected to the base of the transistor 610 via a diode 615 and a resistor 616, and the collector of the transistor 611 is dc connected to the base of the transistor 610 via a diode 617 and a resistor 618.

The phase-advanced sinusoidal signal corresponding to the input waveform S1 produced by the phase advance unit 6 is connected to the base of the transistor 610 via a shunt diode clipper circuit 619 and a series diode gate 620. The phase-advanced sinusoidal signal corresponding to the input waveform S2 is produced by the phase advance unit 7 and is applied via a shunt diode clipper circuit 621 and series diode 622 to the base of the transistor 611.

A positive-going transition of whichever of the two waveforms is leading in phase causes the corresponding transistor to conduct, and hence the common emitter voltage to rise, cutting off the other transistor. At the same time the collector voltage of the conducting transistor falls, and since this collector is dc coupled to the base of the other transistor, the dc level of the latter transistor base falls relative to its collector to such an extent that it cannot be turned on by the positive-going transition of the waveform which is lagging in phase.

The waveform at the output 9, which is connected to the common emitters of the transistors 610 and 611 is thus a square wave in which the positive and negative transitions correspond to the positive and negative transitions of the one of the signals from the units 6 and 7 which is leading in phase, ie. a square wave which is phase advanced with respect to whichever of the input waveforms S1 and S2 is leading in phase.

The gate unit 10 is illustrated in Fig. 7 and comprises long-tailed pairs 11 and 12. The pair 11 comprises transistors 701 and 702 and the pair 12 comprises transistors 704 and 705, each pair being provided with a respective tail transistor 703 or 705, arranged as constant current sources. Conveniently the transistors 701–706 inclusive are incorporated in an integrated circuit such as the R.C.A. Type CA3054.

A potential divider chain indicated generally by the reference numeral 707 provides means for biassing the transistors 701, 702, 704 and 705 so that, under no signal conditions, the transistors 701 and 705 are conducting and the transistors 702 and 704 are just cut off.

The sense waveform from the generator unit 7 is applied to inputs 11b and 12a, i.e. to the bases of the transistors 702 and 704. The first pulse train from output 2d of the comparator unit 2 is applied to the input 11a, i.e. to the base of the transistor 701, and the second pulse train from the output 2d of the comparator unit 2 is applied to the input 12d, i.e. to the base of the transistor 705. An output 11d is taken from the collector of the transistor 702 and an output 12d is taken from the collector of the transistor 705.

Since the sense waveform is applied to transistors which are biassed to cut-off, no component of this waveform appears at the outputs. However, pulses of the first pulse train which occur during positive half-cycles of the sense waveform appear at the output 11d, and pulses of the second pulse train which occur during positive half-cycles of the sense waveform appear at the output 12d.

Input waveforms to the first long-tailed pair 11 are shown in Fig. 3 at 306 for the case where S1 leads S2, the sense waveform being shown in chain-dotted line. It will be seen that the pulses of the first pulse train occur within the positive half-cycles of the sense waveform. The resulting waveform at the output 11d is shown at 308.

The input waveforms to the second long-tailed pair 12 are shown at 307, from which it is seen that the pulses of the second pulse train fall within negative half-cycles of the sense waveform. Hence no pulse signals appear at the output 12d, as shown at 309.

Corresponding waveforms for the case where S2 leads S1 are shown in Fig. 4 at 406 to 409 inclusive. In this case, pulses of the first pulse train fall within negative half-cycles of the sense waveform and there is no signal at output 11d, while pulses of the second pulse train occur within positive half-cycles of the sense waveform, and therefore appear at the output 12d. Since the input connections to the second long-tailed pair 12 are reversed as compared to the input connections to the first long-tailed pair 11, the pulses appearing at the output 12d of the second pair when S2 leads S1 are of opposite polarity to the pulses appearing at the output 11d of the first pair when S1 leads S2, thus providing a means of determining the sense of the phase difference between the waveforms S1 and S2.

The amplifiers 13 and 14, the integrator 15, the limiter 16 and the double pulse detector unit 17 will be now described with reference to Fig. 8.

The amplifiers 13 and 14 together comprise a dual channel amplifying arrangement, balanced with respect to earth, so as to amplify equally the negative going pulses from the output 11d of the gate unit 10 received at the input terminal 801 of the amplifier 13 and the positive going pulses from the output 12d

of the gate unit 10 received at the input terminal 802 of the amplifier 14. The amplifiers 13 and 14 include respective emitter-follower output stages 803 and 804 so as to produce low output impedances. The emitters of transistors 803 and 804 are connected to respective output terminals 805 and 806 via blocking capacitors and respective d.c. restoration circuits 824 and 825.

When S1 leads S2 in phase, positive-going pulses of constant amplitude and width dependent on the magnitude of the phase difference appear at the output terminal 805 of the amplifier 13, and no signal appears at the output terminal 806 of the amplifier 14, whereas when S2 leads S1, no signal appears at the output terminal 805, and negative-going pulses, also of constant amplitude equal to that of the said positive-going pulses and of width dependent on the magnitude of the phase difference appear at the output terminal 806.

The output terminals 805 and 806 are connected respectively to input terminals 807 and 808 of the balanced integrator unit 15, which therefore produces at its output terminal 809 a positive potential representative of the phase difference when S1 leads S2, and a negative potential representative of the phase difference when S2 leads S1. The output 809 of the integrator unit 15 is connected to an input terminal 810 of a limiter unit 16 comprising a shunt diode clipper circuit 811 arranged to limit the maximum positive and negative excursions of the integrator output potential.

The output terminals 805 and 806 of the amplifiers 13 and 14 are further connected to respective input terminals 812 and 813 of a double-pulse detector unit 17.

The unit 17 comprises a long-tailed transistor pair 814 and 815 with tail transistor 816. The bases of the transistors 814 and 815 are biassed by means of a potential divider chain indicated generally by the reference numeral 817 so that under no signal conditions the transistor 814 is cut off and 815 is conductive. The arrangement is such that the application of a positive-going pulse from the amplifier 13 to the base of the transistor 814 via the input terminal 812, the diode 818 and the voltage reference diode 819 is insufficient to overcome the threshold bias conditions. Similarly, the application of a negative-going pulse from the amplifier 13 to the base of the transistor 815 via the diode 820 is insufficient to overcome the initial bias conditions. Application of both pulses simultaneously will however overcome the bias conditions so that transistor 815 becomes cut off and 814 becomes conductive. The collector of the transistor 815 then goes positive. Since the collector of the transistor 815 is dc coupled to the base of the transistor 814 through the resistor 821, the transistor 815 remains cut off so long as pulses are being received simultaneously at the input terminals 812 and 813.

The collector of the transistor 815 is connected via voltage reference diode 822 and a diode 823 to the input terminal 810 of the limiter circuit 16. When the transistor 815 is conductive, the potential of its collector is insufficient to cause the voltage reference diode 822 to conduct, and the limiter 16 receives only the output signal from the integrator 15.

When the transistor 815 is cut off, its collector potential rises sufficiently to cause the voltage reference diode 822 to become conductive, A positive potential is then applied to the limiter 16, such that its output is held at a constant positive level for all phase differences sufficiently great to cause pulses to appear simultaneously at the outputs 11d and 12d of the gate unit 10, i.e. for phase differences typically greater than $\pm 135°$.

In a typical experiment, the embodiment described hereinbefore was employed to measure the phase difference between two sinusoidal signals having a frequency of 4.43MHZ, i.e. colour subcarrier signals for a PAL colour TV system. The results obtained are shown in Fig. 5, from which it may be seen that for phase differences between $-125°$ through zero to $+125°$, the signal at the output of the limiter 16 varied from -1.2V through zero to $+1.2$V, and for phase differences between $+125°$ through $180°$ to $-125°$, at which phase differences double-pulsing occurred, the output was held constant at $+1.40$ volts.

The input signals were then changed to have a frequency of 3.5 MHz, the colour subcarrier frequency for an NTSC colour TV system. The apparatus was not changed, modified or adjusted in any way. Operation of the apparatus was not affected and no change could be detected in the output voltage versus phase difference curve. These results indicate that phase comparison apparatus according to the present invention is capable of measuring phase differences over a range of substantially greater than $\pm 100°$, and that its accuracy is not affected by changes of input frequency over a substantial range.

Although the invention has been described herein in relation to its application in synchronising apparatus for television transmission systems, it is to be understood that it is not restricted to such application, and that apparatus according to the invention may be employed for measuring the phase difference between any two alternating signals of similar frequencies.

CLAIMS

1. Apparatus for comparing the phases of first and second alternating signals comprising comparator means for producing a first pulse train of which successive pulses correspond in

width to the time intervals between corresponding zero crossings in a first sense of successive cycles of the first and second signals and a second pulse train of which successive pulses correspond in width to the time intervals between corresponding zero crossings in an opposite sense of successive cycles of the first and second signals, the pulses of the first pulse and the pulses of the second pulse train being of equal amplitudes and the same polarity, means for generating a substantially square sense waveform corresponding in phase to the one of the first and second signals which is leading in phase, means for gating the first pulse train and the second pulse train by the sense waveform to produce a gated first pulse train only when the phase of the first signal is in advance of the phase of the second signal and to produce a gated second pulse train having pulses of polarity opposite to the pulses of the gated first pulse train only when the phase of the second signal is in advance of the phase of the first signal and means for integrating either the pulses of the gated first pulse train or the pulses of the gated second pulse train to produce a dc output signal whose magnitude and polarity are representative respectively of the magnitude and sense of the phase difference between the first and second signals.

2. Apparatus according to Claim 1 in which the comparator means comprises a first and a second long-tailed pair transistor circuit so arranged that under no-signal conditions a first transistor of the first pair and a first transistor of the second pair are conductive, a second transistor of the first pair and a second transistor of the second pair being non-conducting, the first alternating signal being connected to the respective base electrodes of the first transistor of the first pair and the second transistor of the second pair, the second alternating signal being connected to the respective base electrodes of the second transistor of the first pair and the first transistor of the second pair, the first pulse train being obtained at a collector electrode of the second transistor of the first pair and the second pulse train being obtained at a collector electrode of the first transistor of the second pair.

3. Apparatus according to Claim 1 or Claim 2 in which the means for generating the sense waveform comprises a bistable circuit having first and second trigger inputs, a first trigger signal corresponding to the first alternating signal being connected to the first trigger input and a second trigger signal corresponding to the second alternating signal being connected to the second trigger input, the arrangement being such that when the circuit is set to a particular state by a transition in one sense of either one of the trigger signals, it remains in that state until reset to its other stable state by a transition in the opposite sense of the same trigger signal, irrespective of any changes in the other trigger signal in the intervening period.

4. Apparatus according to Claim 4 further comprising means for advancing the phase of the first trigger signal with respect to the phase of the first alternating signal and means for advancing the phase of the second trigger signal with respect to the phase of the second alternating signal.

5. Apparatus according to any of Claims 1 to 4 in which the means for gating the first pulse train and the second pulse train with the sense waveform comprises a first and a second long-tailed pair transistor circuit so arranged that under no-signal conditions a first transistor of the first pair and a second transistor of the second pair are conducting, a second transistor of the first pair and a first transistor of the second pair being non-conducting, the first pulse train being connected to a base electrode of the first transistor of the first pair, the second pulse train being connected to a base electrode of the second transistor of the second pair and the sense waveform being connected to respective base electrodes of the second transistor of the second pair and the first electrode of the first pair, the gated first pulse train being obtained at a collector electrode of the second transistor of the first pair and the gated second pulse train being obtained at a collector electrode of the second transistor of the second pair.

6. Apparatus according to any preceding Claim further comprising means for detecting the simultaneous occurrence of pulses of the gated first pulse train and of the gated second pulse train and for over-riding the output signal from the integrator means when such simultaneous pulses are detected.

7. Apparatus for comparing the phases of first and second alternating signals substantially as hereinbefore described with reference to the accompanying drawings.

8. Apparatus according to any preceding Claim operatively connected in a colour television transmission system.

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